PRODUCT / PROCESS CHANGE NOTIFICATION

1. PCN basic data	
1.1 Company	STMicroelectronics International N.V
1.2 PCN No.	EMBEDDED PROCESSING/26/16335
1.3 Title of PCN	ST Shenzhen (China) matte Tin post plating introduction for 1Kb to 128Kb I²C EEPROM in SO8N
1.4 Product Category	Low densities EEPROM I²C in SO8N from 1Kb to 128Kb.
1.5 Issue date	2026-05-13

2. PCN Team	
2.1 Contact supplier	
2.1.1 Name	
2.1.2 Phone	
2.1.3 Email	
2.2 Change responsibility	
2.2.1 Product Manager	
2.1.2 Marketing Manager	
2.1.3 Quality Manager	

3. Change		
3.1 Category	3.2 Type of change	3.3 Manufacturing Location
Materials	New direct material part number (same supplier, different supplier or new supplier), Lead frame finishing material / area (internal)	N/A

4. Description of change		
	Old	New
4.1 Description	The low densities EEPROM I²C from 1Kb to 128Kb, processed with the CMOS F8H+ technology, currently assembled in SO8N at ST Shenzhen (China) with NiPdAgAu pre-plated frame...	...will be now assembled with matte Tin post-plated frame.
4.2 Anticipated Impact on form,fit, function, quality, reliability or processability?	- Form: Matte appearance of leads compared to NiPdAgAu pre-plated leadframe - Fit: No change - Function: No change	

5. Reason / motivation for change	
5.1 Motivation	The strategy of the STMicroelectronics Memory division is to support our customers on products and service quality on a long-term basis. In line with this commitment, the qualification of the matte Tin post-plating at ST Shenzhen will allow us to increase capacity and reinforce long term competitiveness. For optimal service and security of double sourcing, this PCN is coupled with the TSHT PCN (16143 & 16334).
5.2 Customer Benefit	DOUBLE SOURCING

6. Marking of parts / traceability of change	
6.1 Description	N/A

7. Timing / schedule	
7.1 Date of qualification results	2026-07-06
7.2 Intended start of delivery	2026-08-10
7.3 Qualification sample available?	Upon Request

8. Qualification / Validation	
8.1 Description	16335 RRCS2522 Reliability report F8H SO8N SHZ Postplating.pdf

8.2 Qualification report and qualification results	Available (see attachment)	Issue Date	2026-05-13

9. Attachments (additional documentations)
16335 Public product.pdf 16335 PCN TIN PLATING SO8 SHENZHEN.pdf 16335 RRCS2522 Reliability report F8H SO8N SHZ Postplating.pdf

10. Affected parts		
10. 1 Current		10.2 New (if applicable)
10.1.1 Customer Part No	10.1.2 Supplier Part No	10.1.2 Supplier Part No
	M24128-BFMN6TP	
	M24128-BRMN6TP	
	M24128-BWMN6TP	
	M24C01-RMN6TP	
	M24C01-WMN6TP	
	M24C02-FMN6TP	
	M24C02-RMN6TP	
	M24C02-WMN6TP	
	M24C04-FMN6TP	
	M24C04-RMN6TP	
	M24C04-WMN6TP	
	M24C08-FMN6TP	
	M24C08-RMN6TP	
	M24C08-WMN6TP	
	M24C16-FMN6TP	
	M24C16-RMN6TP	
	M24C16-WMN6TP	
	M24C32-FMN6TP	
	M24C32-RMN6TP	
	M24C32-WMN6TP	
	M24C64-FMN6TP	
	M24C64-RMN6TP	
	M24C64-WMN6TP	

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Public Products List

Publict Products are off the shelf products. They are not dedicated to specific customers, they are available through ST Sales team, or Distributors, and visible on ST.com

PCN Title : ST Shenzhen (China) matte Tin post plating introduction for 1Kb to 128Kb I²C EEPROM in SO8N

PCN Reference : EMBEDDED PROCESSING/26/16335

Subject : Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change.

M24128-BFMN6TP	M24C04-RMN6TP	M24C02-FMN6TP
M24128-BRMN6TP	M24C64-WMN6TP	M24C32-RMN6TP
M24C04-WMN6TP	M24C01-RMN6TP	M24C32-WMN6TP
M24C08-FMN6TP	M24C16-FMN6TP	M24C64-FMN6TP
M24C02-WMN6TP	M24C08-WMN6TP	M24128-BWMN6TP
M24C32-FMN6TP	M24C16-RMN6TP	M24C16-WMN6TP
M24C64-RMN6TP	M24C01-WMN6TP	M24C08-RMN6TP
M24C02-RMN6TP	M24C04-FMN6TP	

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PRODUCT / PROCESS CHANGE NOTIFICATION

ST Shenzhen (China) matte Tin post plating introduction for 1Kb to 128Kb I²C EEPROM in SO8N

What is the change?
The **low densities EEPROM I²C** from **1Kb to 128Kb**, processed with the CMOS F8H+ technology, currently assembled in SO8N at **ST Shenzhen (China)** with NiPdAgAu pre-plated frame **will be now assembled with matte Tin post-plated frame**.

Why?
The strategy of STMicroelectronics is to support our customers on products and service quality on a long-term basis. In line with this commitment, the qualification of the matte Tin post-plating at ST Shenzhen will allow us to increase capacity and reinforce long term competitiveness.
For optimal service and security of double sourcing, this PCN is coupled with the TSHT additional back-end PCNs (16143 & 16334).

When?
Qualified samples will be available from Week 28 / 2026.
Shipment will start from Week 33 / 2026 or earlier depending on customer agreement.

How will the change be qualified?
This change is qualified using the standard STMicroelectronics Corporate Procedures for Quality and Reliability.
The intermediate Reliability Evaluation Report **RRCS2522** is available.
The final Reliability Evaluation Report **RRCS2522** will be available Week 28 / 2026.

What is the impact of the change?
- **Form: Matte appearance of leads** compared to NiPdAgAu pre-plated leadframe
- **Fit:** No change
- **Function:** No change

- ***BOX LABEL MARKING***

On the BOX LABEL, the difference is visible inside the **Finished Good Part Number** where the "**Assembly plant**" identifier is "**SA**" for products assembled with **matte Tin post-plating** frame, this identifier being "HA" for current products assembled with NiPdAgAu pre-plated frame.

Example for M24C64-RMN6TP

- VISUAL APSPECT

Matte Tin post-plating is showing the leads with a **matte appearance and silver color** while the pre-plated leads with NiPdAgAu are more shiny with a very light golden color.

ST Shenzhen matte Tin post-plating

ST Shenzhen NiPdAgAu pre-plating

Appendix A- Product Change Information

Product family / Commercial products:	Low densities EEPROM I²C in SO8N from 1Kb to 128Kb.
Customer(s):	All
Type of change:	Lead plating change
Reason for the change:	Double sourcing
Description of the change:	Matte Tin post-plating at ST Shenzhen (China)
Forecast date of the change: (Notification to customer)	Week 20 / 2026
Forecast date of Qualification samples availability for customer(s):	Week 28 / 2026
Qualification Report availability:	The Intermediate Reliability Evaluation Report **RRCS2522** is available. The final Reliability Evaluation Report **RRCS2522** will be available Week 28 / 2026.
Marking to identify the changed product:	N/A
Description of the qualification program:	Standard ST Microelectronics Corporate Procedures for Quality and Reliability
Estimated date of first shipment:	Week 33 / 2026 or earlier on customer agreement

Appendix B: BOM comparison:

	New ST Shenzhen	Current ST Shenzhen
Leadframe	**Matte Tin post plating**	PPF 4-layer NiPdAgAu
Molding compound	**HHCK EMG-600**	SUMITOMO G700K
Glue die-attach	**ABLESTIK 8601S** (PFAS free)	ABLESTIK 8611
Wire	**Cu**	Cu

Appendix B: concerned Commercial Part Numbers:

Commercial product	Finished Good Part number	Qualified samples availability
M24C01-RMN6TP	M24C01-RMN6TPTSA	Week 28 / 2026
M24C01-WMN6TP	M24C01-WMN6TPTSA	Week 28 / 2026
M24C02-FMN6TP	M24C02-FMN6TPTSA	Week 28 / 2026
M24C02-RMN6TP	M24C02-RMN6TPTSA	Week 28 / 2026
M24C02-WMN6TP	M24C02-WMN6TPTSA	Week 28 / 2026
M24C04-FMN6TP	M24C04-FMN6TPTSA	Week 28 / 2026
M24C04-RMN6TP	M24C04-RMN6TPTSA	Week 28 / 2026
M24C04-WMN6TP	M24C04-WMN6TPTSA	Week 28 / 2026
M24C08-FMN6TP	M24C08-FMN6TPTSA	Week 28 / 2026
M24C08-RMN6TP	M24C08-RMN6TPTSA	Week 28 / 2026
M24C08-WMN6TP	M24C08-WMN6TPTSA	Week 28 / 2026
M24C16-FMN6TP	M24C16-FMN6TPTSA	Week 28 / 2026
M24C16-RMN6TP	M24C16-RMN6TPTSA	Week 28 / 2026
M24C16-WMN6TP	M24C16-WMN6TPTSA	Week 28 / 2026
M24C32-FMN6TP	M24C32-FMN6TPTSA	Week 28 / 2026
M24C32-RMN6TP	M24C32-RMN6TPTSA	Week 28 / 2026
M24C32-WMN6TP	M24C32-WMN6TPTSA	Week 28 / 2026
M24C64-FMN6TP	M24C64-FMN6TPTSA	Week 28 / 2026
M24C64-RMN6TP	M24C64-RMN6TPTSA	Week 28 / 2026
M24C64-WMN6TP	M24C64-WMN6TPTSA	Week 28 / 2026
M24128-BFMN6TP	M24128BFMN6TPTSA	Week 28 / 2026
M24128-BRMN6TP	M24128BRMN6TPTSA	Week 28 / 2026
M24128-BWMN6TP	M24128BWMN6TPTSA	Week 28 / 2028

Document Revision History

Date	Rev.	Description of the Revision
May 11, 2026	1.00	Christian POLI - First draft creation

Source Documents & Reference Documents

Source document Title	Rev.:	Date:

RRCS2522 - Reliability Report

Bill of Material and Process Change

F8H+ SO8N SHZ Postplating

General Information	
Commercial Product	M24C08-WMN6TP, M24128-BFMN6TP, M24C08-FMN6TP, M24C08-RMN6TP, M24128-BRMN6TP, M24128-BWMN6TP
Product Line	24081T,24281T
Package	SO 08 .15 JEDEC
Silicon Technology	CMOSF8H+

Traceability	
Diffusion Plant	Rousset 8
Assembly Plant	SHZ – Shenzhen - China

Reliability Assessment	
Pass	x
Fail	

Release	Date	Author	Function
1.0	May 5th 2026	Michel DERIE	CS Back-End quality Manager

DOCUMENT ACTORS:

Name	Function	Location	Date
Michel DERIE	CS Back-End quality Manager	Rousset	May 5th 2026
Olivier VALLIER	CS Product Qualification and Reliability Engineer	Rousset	May 5th 2026
Nicolas DUMONT	CS Product Qualification and Reliability Manager	Rousset	May 5th 2026

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RELIABILITY EVALUATION OVERVIEW

- **OBJECTIVE**

The aim of this reliability is to qualify the new version of SO8N package with a cost improved Bill Of Material including Cu wire and Postplated lead frame for F8H+ technology serial EEPROM ICs.

Scope:

- F8H+ technology serial I²C EEPROM products with memory size 1k to 128k.
- Package SO8N
- Wire type Cu

- **CONCLUSION**

All reliability tests concerning 8k product have been completed with positive results. Neither functional nor parametric rejects were detected at final electrical testing.
Package oriented tests have not put in evidence any criticality.

Based on the overall results obtained, F8H+ technology EEPROM products with memory size 8k, assembled in SO8N package using SHZ post plating process have positively passed reliability evaluation.
128k products reliability is still ongoing.

TABLE OF CONTENT

1. RELIABILITY STRATEGY

Reliability evaluation is based on the standard STMicroelectronics corporate procedures for quality and reliability, namely RELIABILITY TESTS AND CRITERIA FOR QUALIFICATION, and in compliance with the JESD-47K international standard.

The following qualification strategy has been defined:

- Package reliability evaluation on 3 assembly lots 8k memory and 3 lots 128k memory of F8H+ technology This will allow to qualify all intermediate memory sizes.
- This report shows the intermediate results of 8k products.

Reliability trials performed as part of this reliability evaluation are listed in test results summary in section 3, including specifications references

2. PRODUCT OR TEST VEHICLE CHARACTERISTICS

2.1. Generalities

The 3 lots used for qualification 1st step are 8k product.
128k product reliability is ongoing.

2.2. Traceability

2.2.1. Wafer Fab Information

Main die - S24081TA

Wafer Fab Information	
FAB1	
Wafer fab name / location	ST SAS Rousset / Rousset 8
Wafer diameter (inches)	8
Wafer thickness (µm)	280
Silicon process technology	CMOSF8H+
Die finishing front side (passivation) materials	USG NitUV (HFP USG UV Nitride)
Die finishing back side Materials	RAW SILICON - BACK GRINDING
Stepping die size (µm)	494, 604
Sawing street width (X,Y) (µm)	60,80

Main die - S24281TA

Wafer Fab Information	
FAB1	
Wafer fab name / location	ST SAS Rousset / Rousset 8
Wafer diameter (inches)	8
Wafer thickness (µm)	280
Silicon process technology	CMOSF8H+
Die finishing front side (passivation) materials	USG NitUV (HFP USG UV Nitride)
Die finishing back side Materials	RAW SILICON - BACK GRINDING
Stepping die size (µm)	968, 856
Sawing street width (X,Y) (µm)	60,80

2.2.2. Assembly information

-Assembly Information	
Package :SO 08 .15 JEDEC	
Assembly plant name / location	Shenzhen - China
Die thickness after back-grinding (µm)	280µ
Die sawing method	Mechanical
Lead frame/Substrate material/supplier/reference	SO8 60x60
Lead frame finishing (material/thickness)	Ag Spot
Die attach material/type(glue/film)/supplier	GLUE LOCTITE ABLESTIK 8601S-25NP
Wire bonding material/diameter/supplier	0.8mil Cu
Molding compound material/supplier/reference	RESIN HHCK EMG-600-2
Package Moisture Sensitivity Level (JEDEC J-STD020D)	MSL1

3. TEST RESULTS SUMMARY

3.1. Reliability testing information

Reliability Testing Information	
Reliability laboratory name / location	Grenoble Rel Lab, Rousset MDG Rel Lab , TSHT reliability lab

Note: ST is ISO 9001 certified. This induces certification of all internal and subcontractor labs. ST certification document can be downloaded under the following link: http://www.st.com/content/st_com/en/support/quality-and-reliability/certifications.html

3.2. Lot information

Lot #	Diffusion Lot	Assy Lot	Raw Line	Package
Lot 1	G520164	GK545QCG01	PSO7*24081TA	SO 08 .15 JEDEC
Lot 2	G520164	GK545QCGRL	PSO7*24081TA	SO 08 .15 JEDEC
Lot 3	G520164	GK545QCGRM	PSO7*24081TA	SO 08 .15 JEDEC

3.3. Test plan and results summary

ACCELERATED ENVIRONMENT STRESS TESTS

Test code	Stress method	Stress Conditions	Lots Qty	S.S.	Total	Results/Lot Fail/S.S.	Comments:(N/A =Not Applicable)
PC	J-STD-020	24h bake@125°C, T&H 168h 85°C/85%RH 3x Reflow simulation Peak Reflow Temp= 260°C ☒ Testing at Room T°	3	231	693	Lot 1 : 0/231 Lot 2 : 0/231 Lot 3 : 0/231	
HTSL	JESD22-A103	Ta= 150°C Duration= 1000h ☒ Testing at Room T°	3	77	231	Lot 1 : 0/77 Lot 2 : 0/77 Lot 3 : 0/77	
TC	JESD22-A104	Ta= -65 / +150°C, 2cy/h Duration = 500cy ☒ After PC ☒ Testing at Room T°	3	77	231	Lot 1 : 0/77 Lot 2 : 0/77 Lot 3 : 0/77	
HAST	JESD22-A118	Ta=130°C/85%RH + bias Vcc max Duration= 96h ☒ After PC ☒ Testing at Room T°	3	77	231	Lot 1 : 0/77 Lot 2 : 0/77 Lot 3 : 0/77	
UHAST	JESD22-A118	Ta=130°C/85%R Duration= 96h ☒ After PC ☒ Testing at Room T°	3	77	231	Lot 1 : 0/77 Lot 2 : 0/77 Lot 3 : 0/77	

Electrical Verification Tests

Test code	Stress method	Stress Conditions	Lots Qty	S.S.	Total	Results/Lot Fail/S.S.	Comments:(N/A =Not Applicable)
CDM	JS-002	3u/ voltage: 250, to 1500V by step of 250V total 18u ☒Testing at Room T°	1	18	18	W28	Gating= 500V

Package Assembly Integrity Tests

Test code	Stress method	Stress Conditions	Lots Qty	S.S.	Total	Results/Lot Fail/S.S.	Comments:(N/A =Not Applicable)
PD	Internal	Dimensions measurement vs POA	3	10	30	PASS	
SD	J-STD-002D	2 conditions ☒ Dry (150°C,8H) SnAgCu ☒ Steam (85 °C/85%RH,8H) SnAgCu	3	20	60	PASS	
WBP	MIL-STD883 Method 2011	EQUIPMENT: Dage BT4000 SAMPLING: 30 wires / 6 units (5 wires /unit) ☒ Testing at T0 after package opening	3	30	90	PASS	
WBS	JESD22-B116	EQUIPMENT: Dage BT4000 SAMPLING: 30 wires / 5 units (6 wires /unit) ☒ Testing at T0 after package opening	3	30	90	PASS	

Note: Test method revision reference is the one active at the date of reliability trial execution.

4. APPLICABLE AND REFERENCE DOCUMENTS

Reference	Short description
JESD47-L	Stress-Test-Driven Qualification of Integrated Circuits

5. GLOSSARY

CDM	Electrostatic Discharge - Charged device model
HAST	Biased HAST (Highly Accelerated Stress Test)
HBM	Electrostatic Discharge - Human Body Model
HTSL	High Temperature Storage Life
PC	Preconditioning
TC	Temperature Cycling
THB	Temperature Humidity Bias
UHAST	Unbiased HAST (Highly Accelerated Stress Test)
WBS	Wire Bond Shear
WBP	Wire Bond Pull
PD	Physical Dimensions
SD	Solderability

6. REVISION HISTORY

Release	Date	Description
1.0	May 5th 2026	Initial release

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